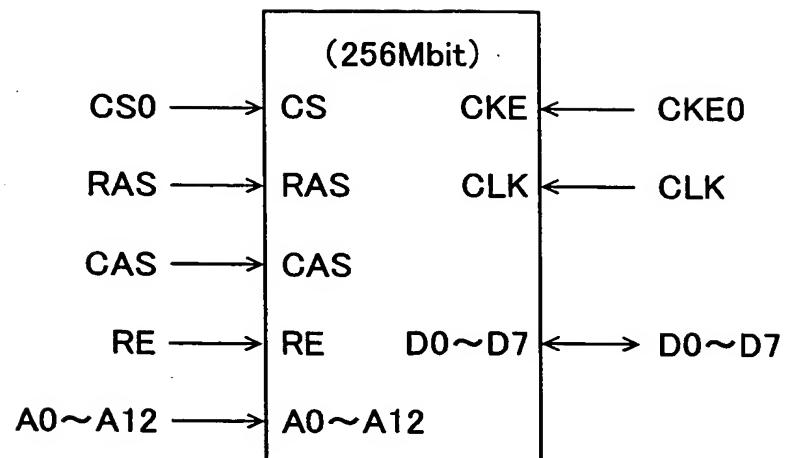


FIG. 1

FIG.2

BANK1



BANK2

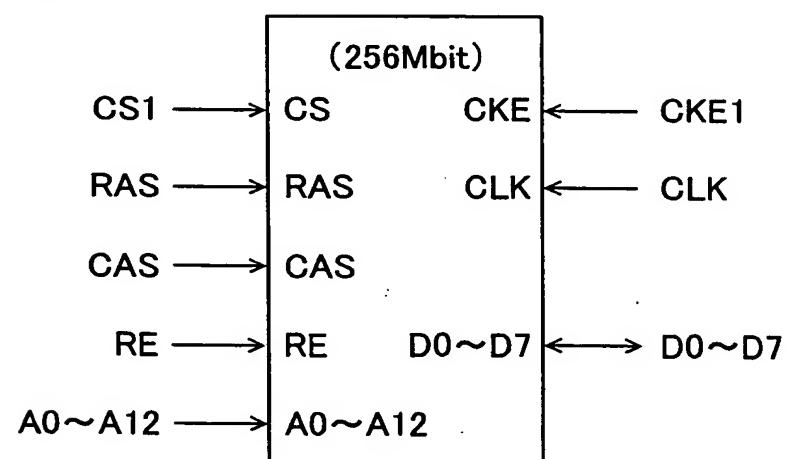
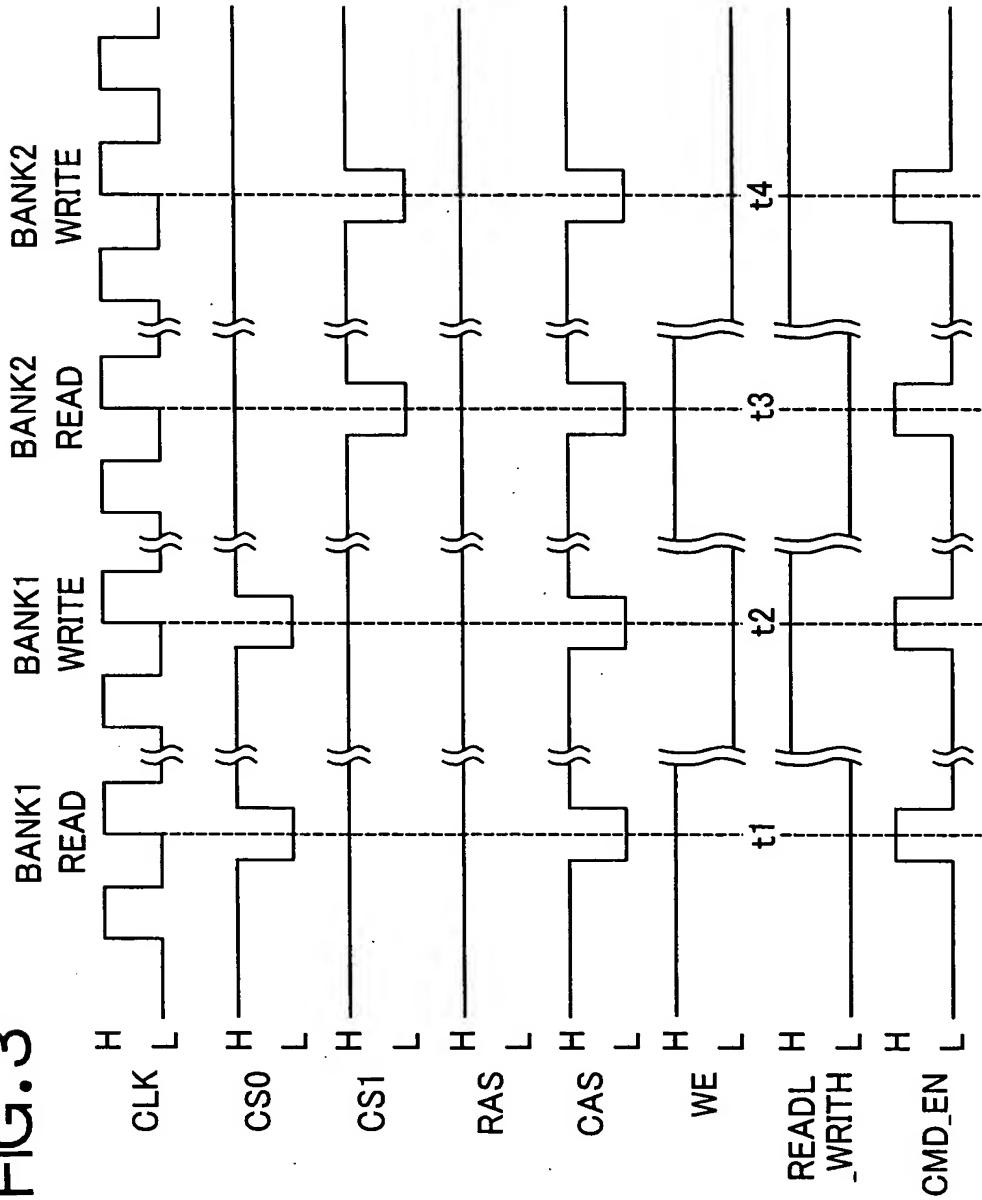


FIG. 3



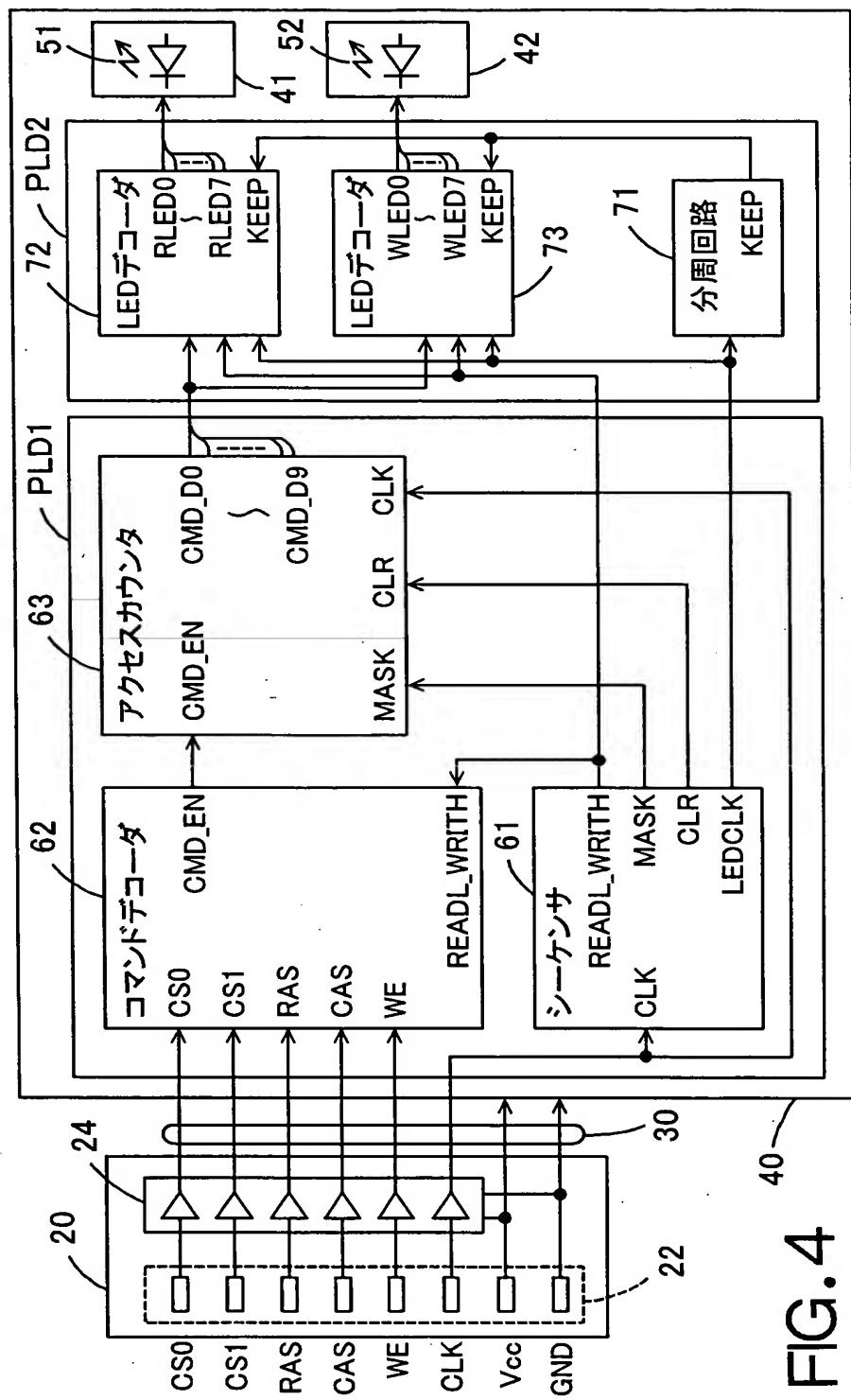


FIG. 4

FIG. 5

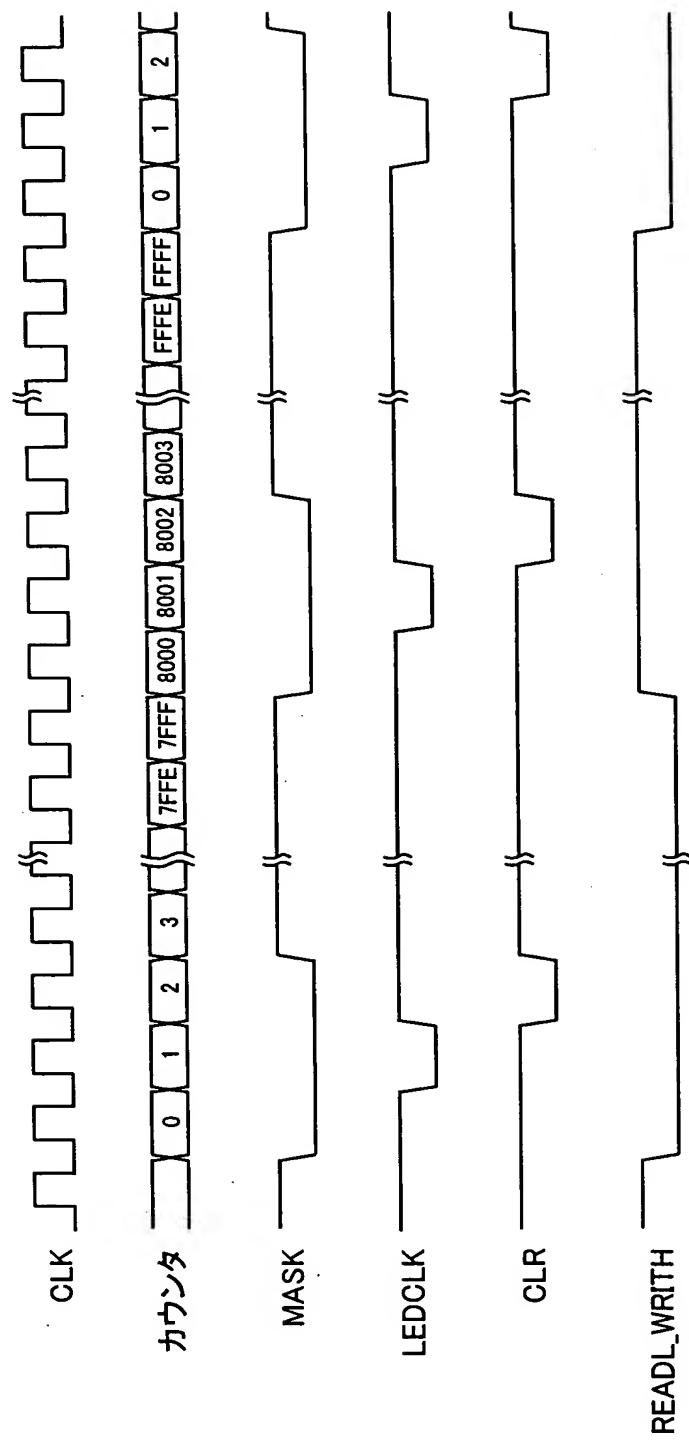


FIG.6

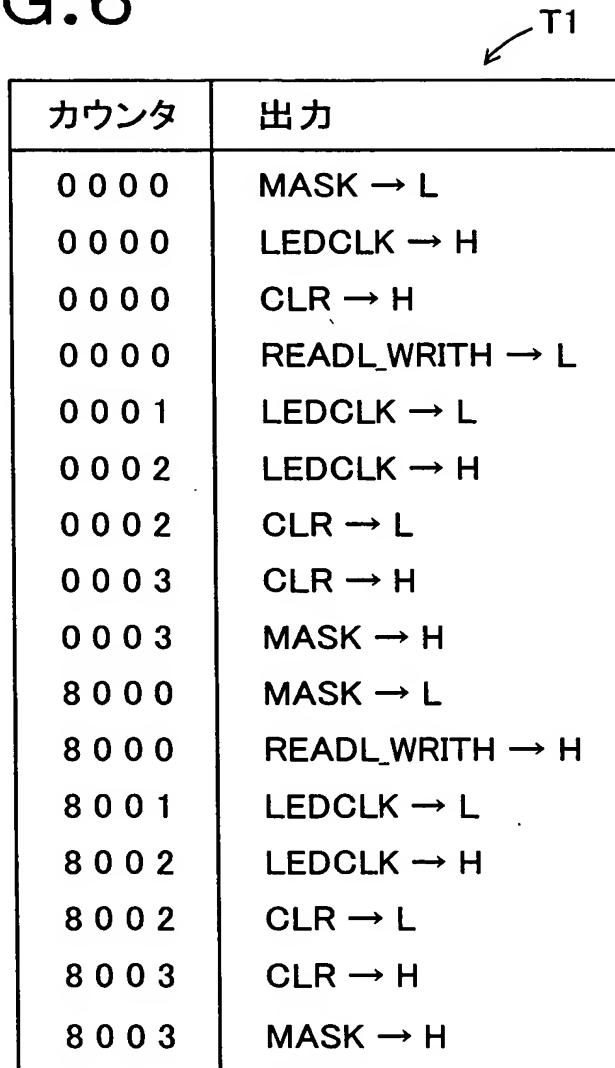


Diagram showing a table with a header row and 16 data rows. The table is labeled T1 with an arrow pointing to its top right corner.

カウンタ	出力
0 0 0 0	MASK → L
0 0 0 0	LEDCLK → H
0 0 0 0	CLR → H
0 0 0 0	READL_WRITH → L
0 0 0 1	LEDCLK → L
0 0 0 2	LEDCLK → H
0 0 0 2	CLR → L
0 0 0 3	CLR → H
0 0 0 3	MASK → H
8 0 0 0	MASK → L
8 0 0 0	READL_WRITH → H
8 0 0 1	LEDCLK → L
8 0 0 2	LEDCLK → H
8 0 0 2	CLR → L
8 0 0 3	CLR → H
8 0 0 3	MASK → H

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FIG. 7

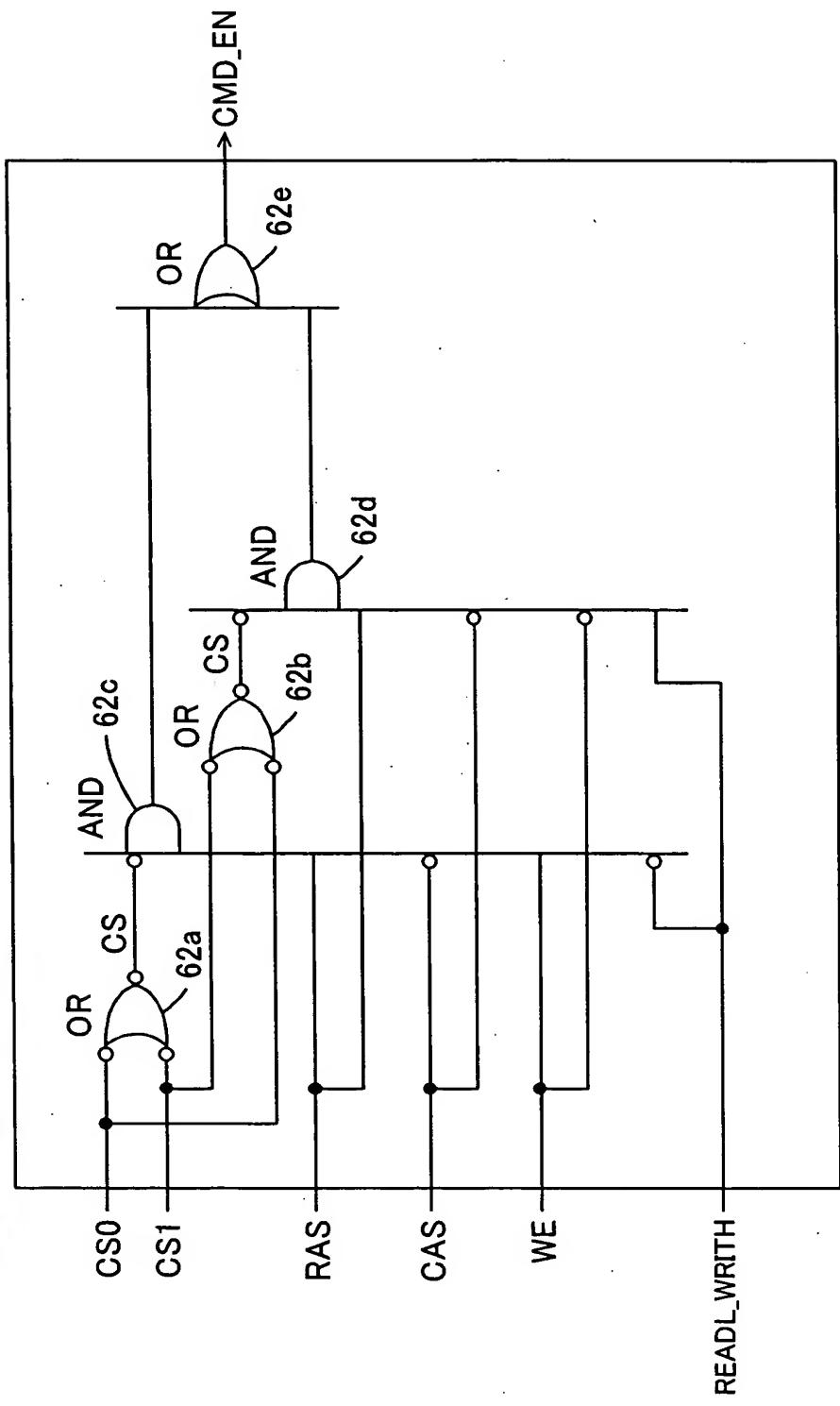


FIG.8

FUNCTION TABLE

入力					出力
CS	RAS	CAS	WE	READL_WRITH	CMD_EN
H	X	X	X	X	L
L	L	X	X	X	L
L	X	H	X	H	L
L	H	L	H	L	H
L	H	L	H	L	L
L	H	H	H	L	L
L	H	H	H	L	L

アクセスカウンタ63

FIG.9

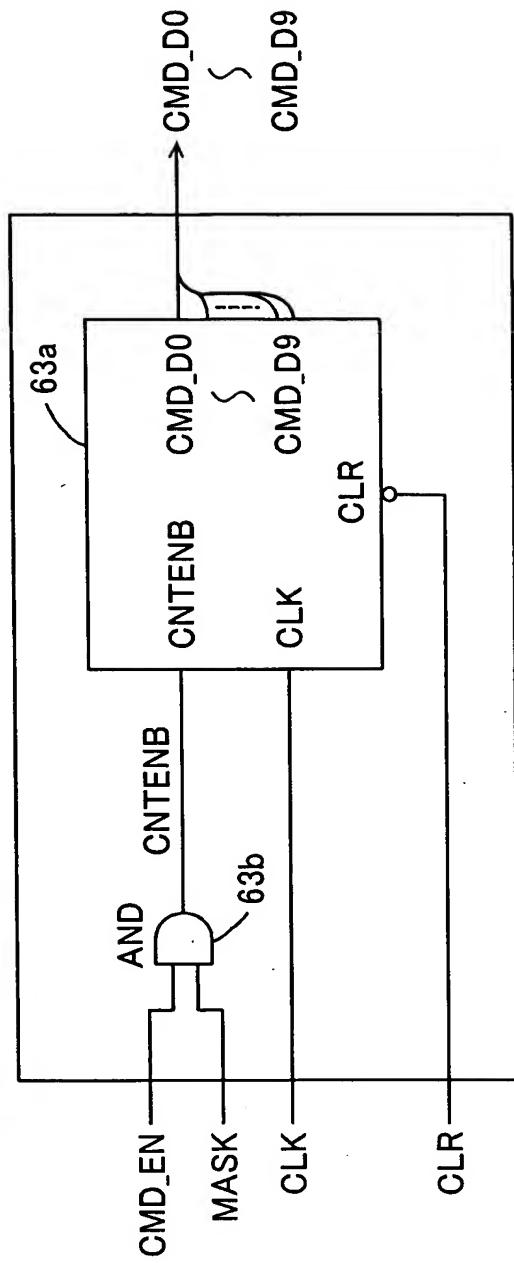


FIG. 10

FUNCTION TABLE

入力				出力
CMD_EN	MASK	CLR	CLK	CMD_D
X	X	L	X	All bit "0"
L	L	H	X	カウント停止
	L	H	X	
	H	H	X	
H	H	H	↑	カウントアップ 0000000000 ← 0000000001 ↓ 1111111110 1111111111

分周回路71

FIG. 11

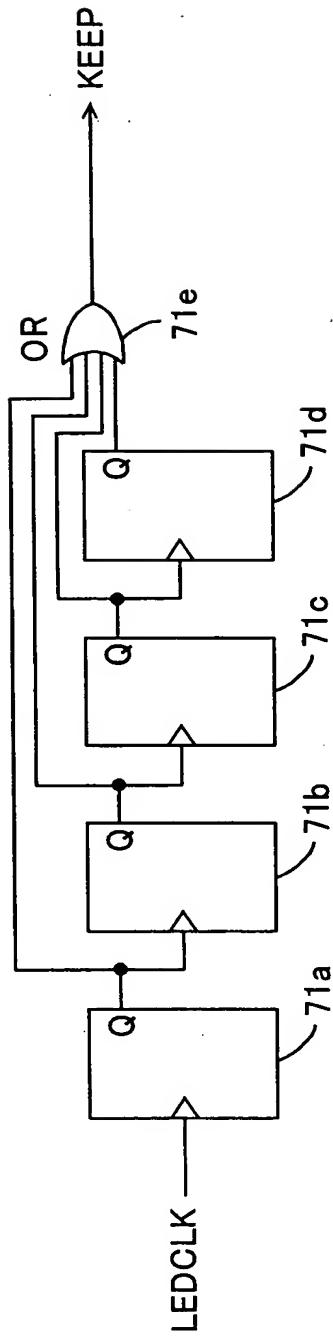


FIG. 12

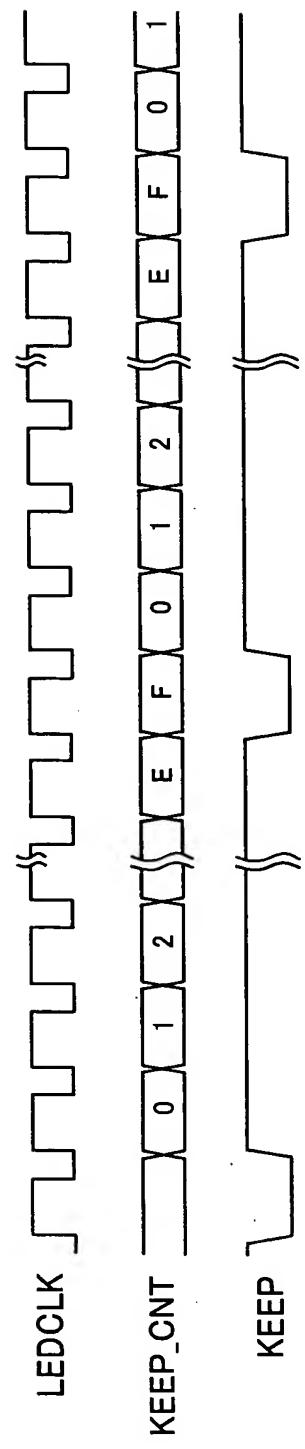


FIG. 13

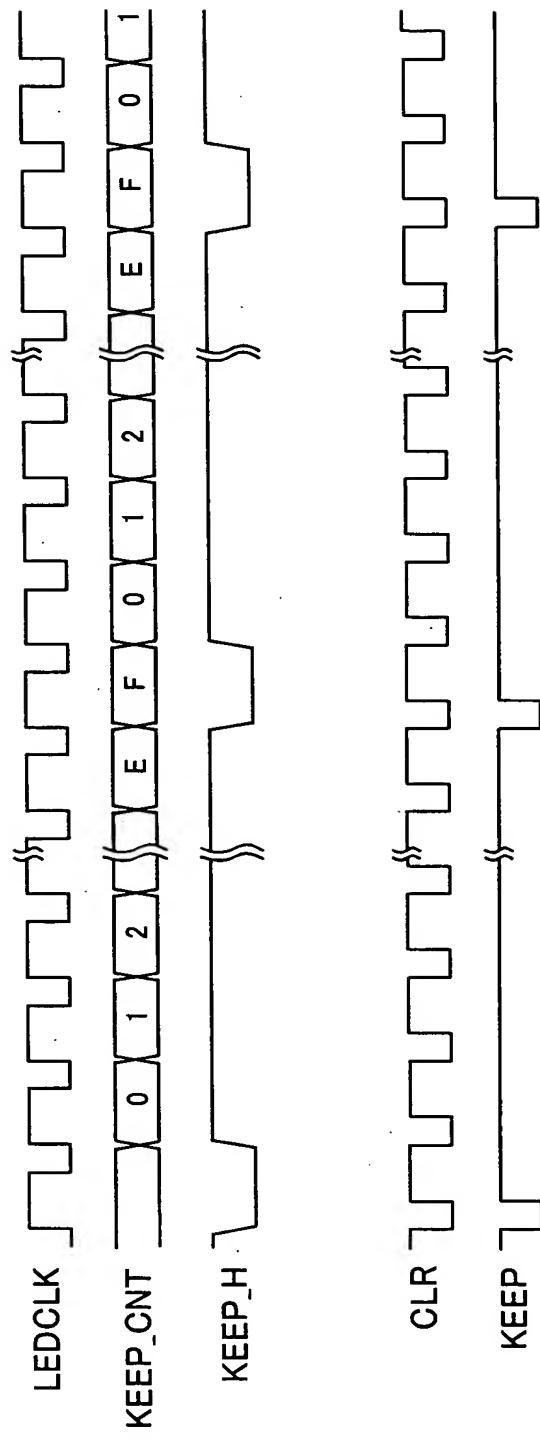


FIG. 14

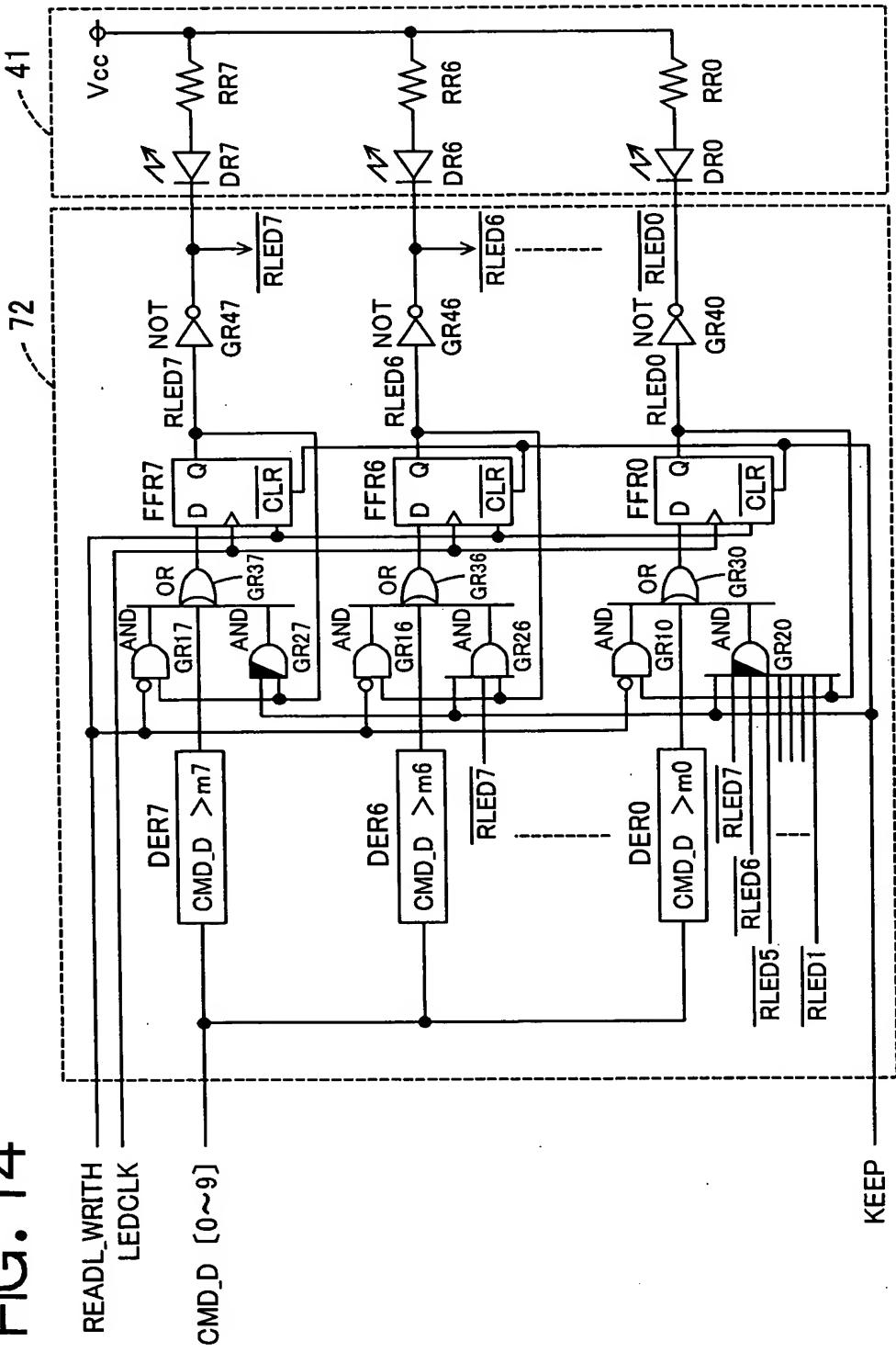


FIG. 15

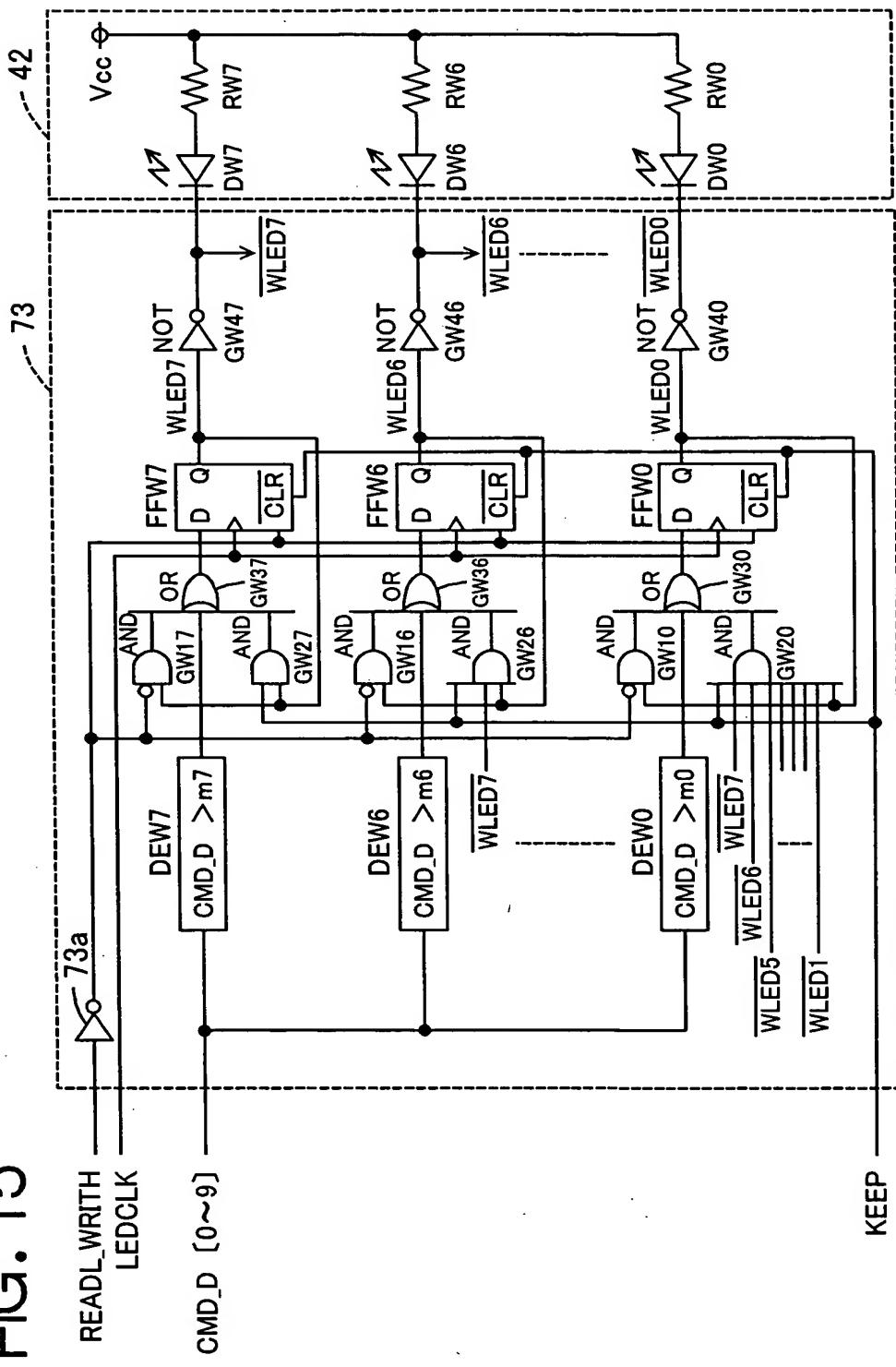
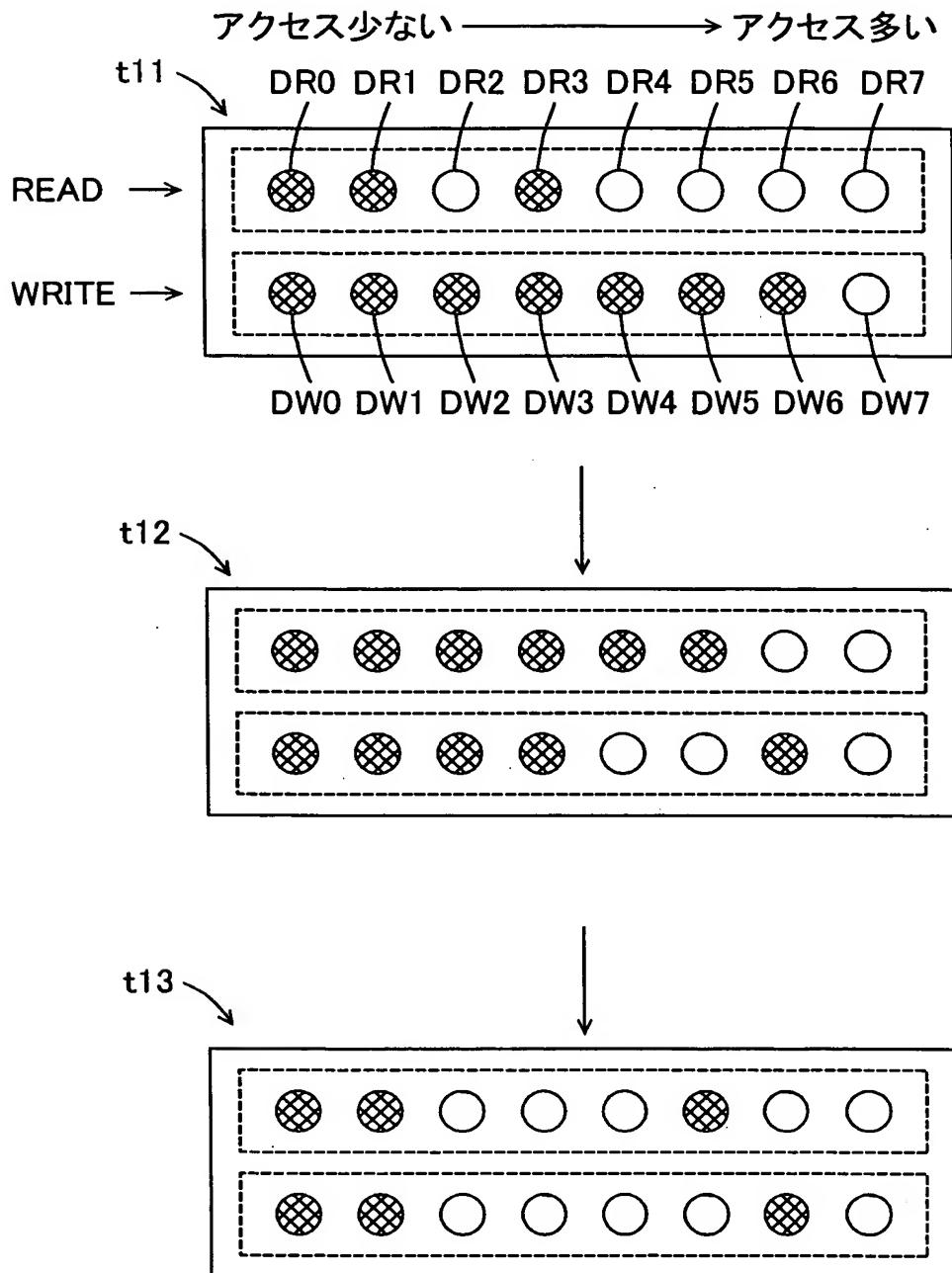


FIG. 16



FUNCTION TABLE

FIG. 17

CMD_D	出力						
	DER0	DER1	DER2	DER3	DER4	DER5	DER6
CMD_D \leqq m0	L	L	L	L	L	L	L
m0 < CMD_D \leqq m1	H	L	L	L	L	L	L
m1 < CMD_D \leqq m2	H	H	L	L	L	L	L
m2 < CMD_D \leqq m3	H	H	H	L	L	L	L
m3 < CMD_D \leqq m4	H	H	H	H	L	L	L
m4 < CMD_D \leqq m5	H	H	H	H	H	L	L
m5 < CMD_D \leqq m6	H	H	H	H	H	H	L
m6 < CMD_D \leqq m7	H	H	H	H	H	H	H
m7 < CMD_D	H	H	H	H	H	H	H

FUNCTION TABLE

FIG. 18

入力						出力	
READL WRITH	DERi	RLEDi	KEEP	<u>RLEDj</u>	LEDCLK	RLEDi	
X	X	X	L	X	X	L	
L	X	X	H	X	X	L	
H	L	L	H	X	X	H	
H	H	X	H	H	X	L	
H	L	H	H	ALL H	X	H	
H	L	H	H	(L)	X	L	

j = i+1 ~ 7

FUNCTION TABLE

FIG. 19

入力					出力	
READL WRITH	DEWI	WLEDi	KEEP	WLEDj	LEDCLK	WLEDi
X	X	X	L	X	X	L
H	X	X	H	X	X	WLEDi
L	L	L	H	X	↑	L
L	H	X	H	X	↑	H
L	L	H	H	H	ALL H	H
L	L	H	H	H	(L)	↑
L	L	H	H	H	↑	L

j = i+1 ~ 7

FIG. 20

